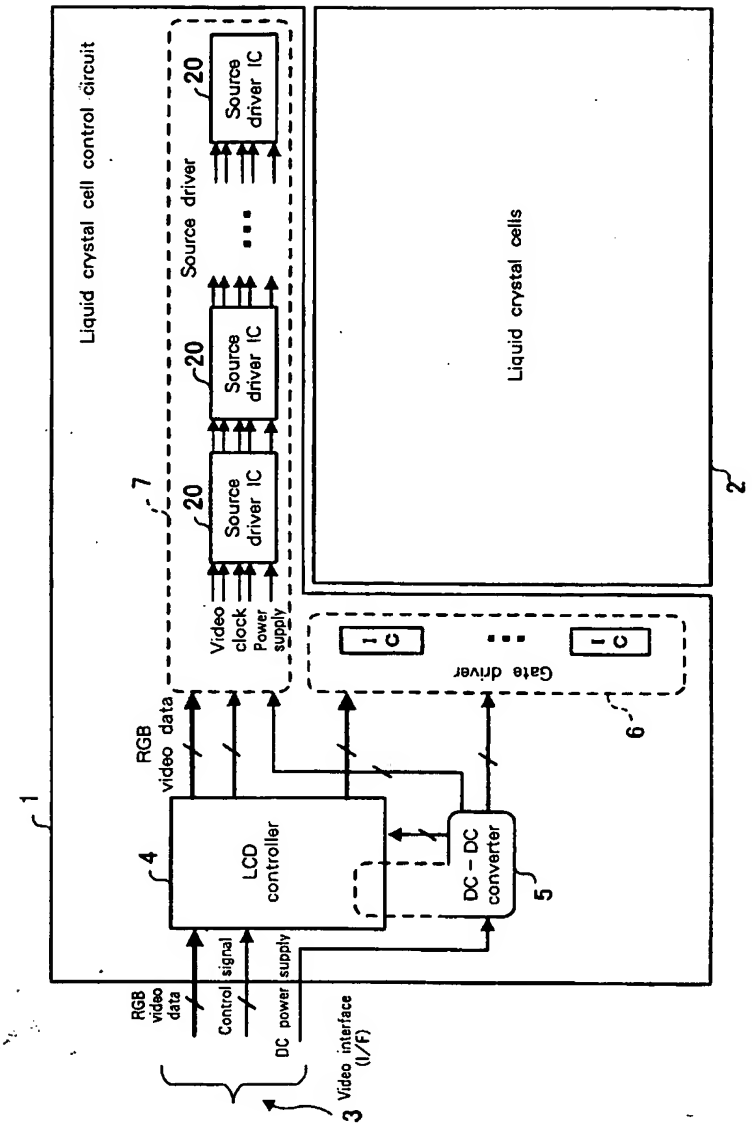
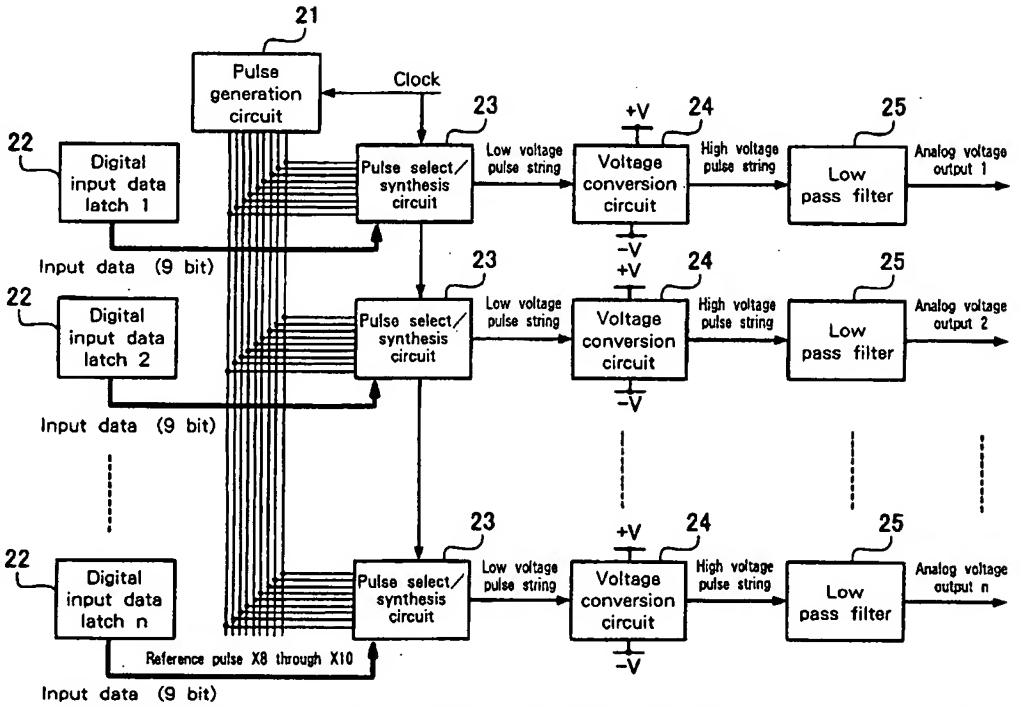
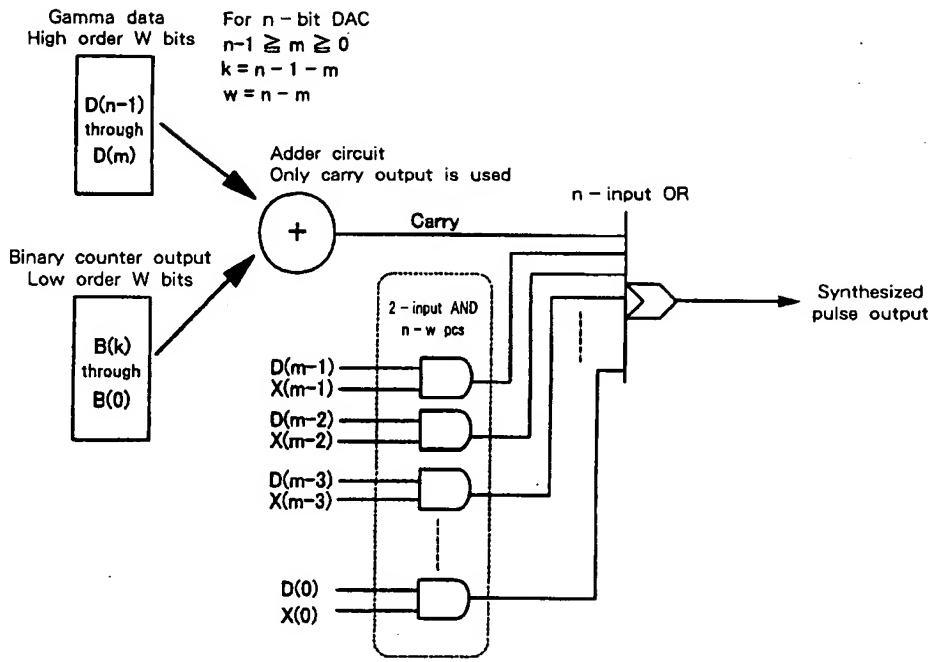


Fig. 1



Configuration for gamma reference voltage generation circuit for LCD source driver

Fig. 2



Details of pulse generation circuit and synthesis circuit for n – bit DAC

Fig. 3

Relationship between the number of divided bits and maximum frequencies of pulse strings when utilizing a pulse generation circuit and pulse synthesis circuit for n – bit DAC

Number of divided bits	Maximum frequency of pulse string (Hz)	Ratio of constant switching frequency range to whole input data	Remarks
W = 1	f	0	PDM
W = 2	f/2	1/2	Minimum circuit scale
W = 3	f/4	3/4	
W = 4	f/8	7/8	
W = 5	f/16	15/16	
-----	-----	-----	
W = n	$f/2^{n-1}$	1	PWM

* Note : Assuming digital input data is n bit

Fig. 4

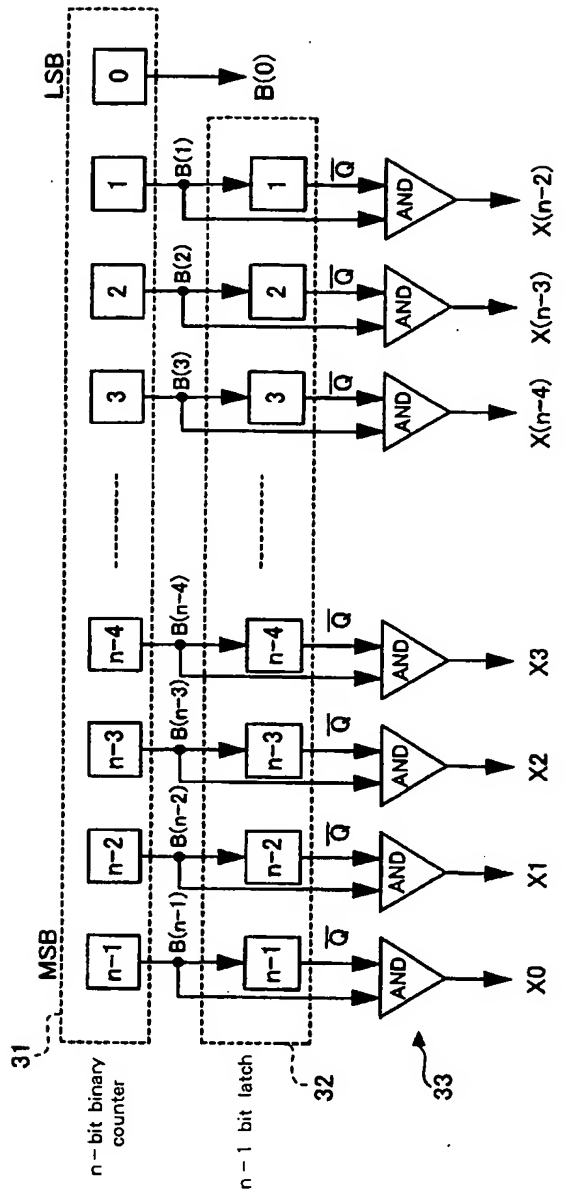


Fig. 5

Typical configuration of pulse generation circuit for PDM type DAC

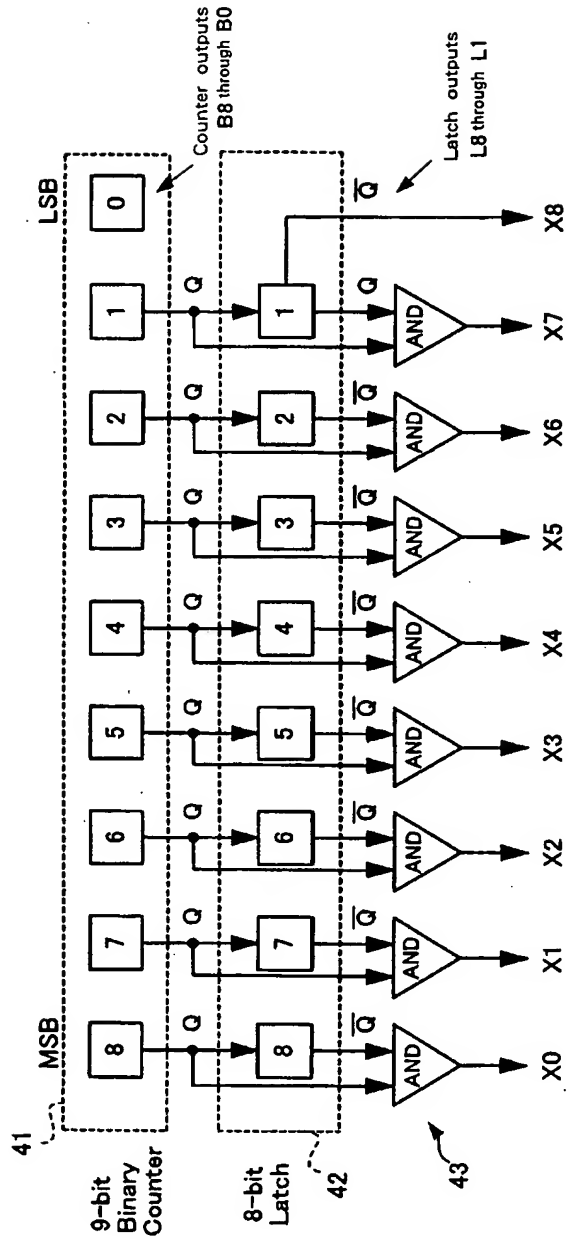
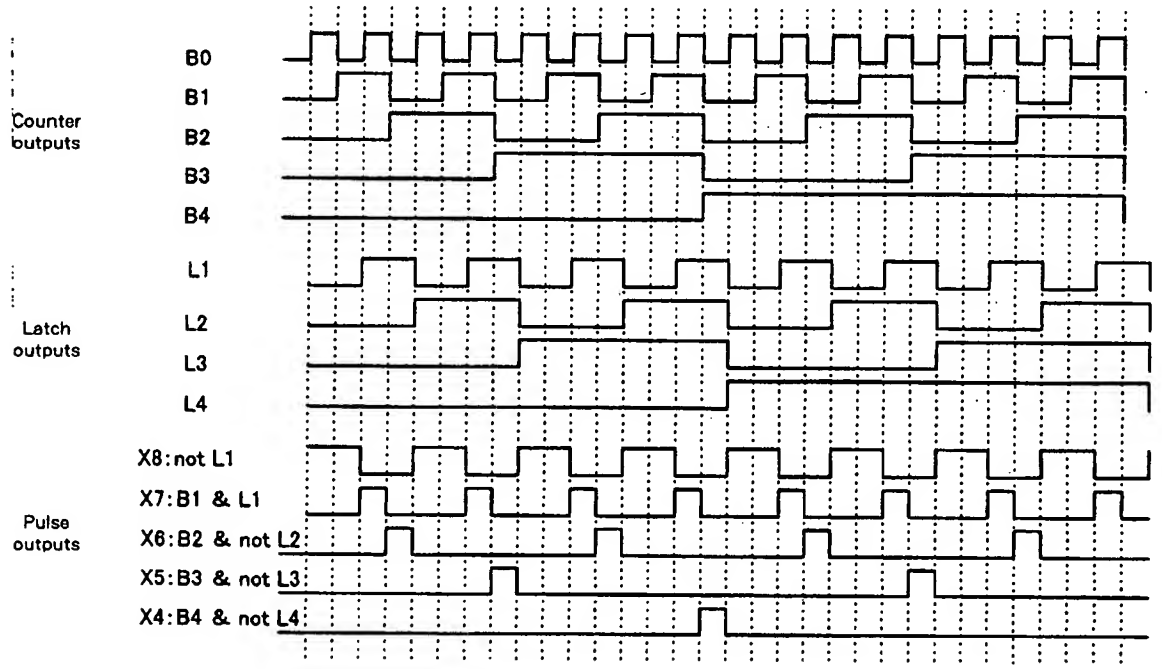
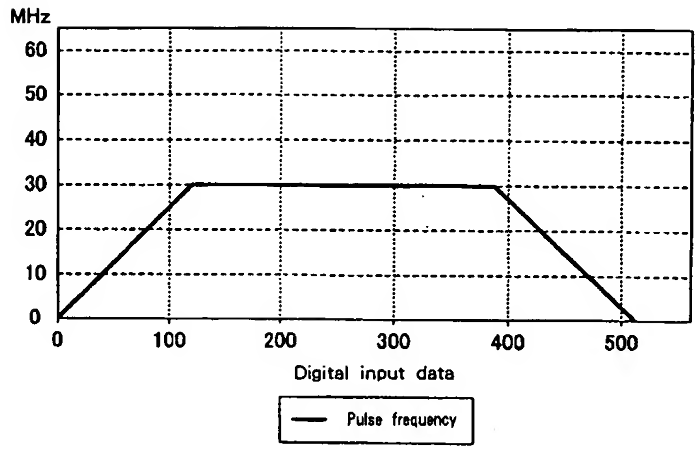


Fig. 6



Example pulse for PDM type DAC

Fig. 7



Relationship between digital input data
and pulse string frequency for pulse generation circuit

Fig. 8

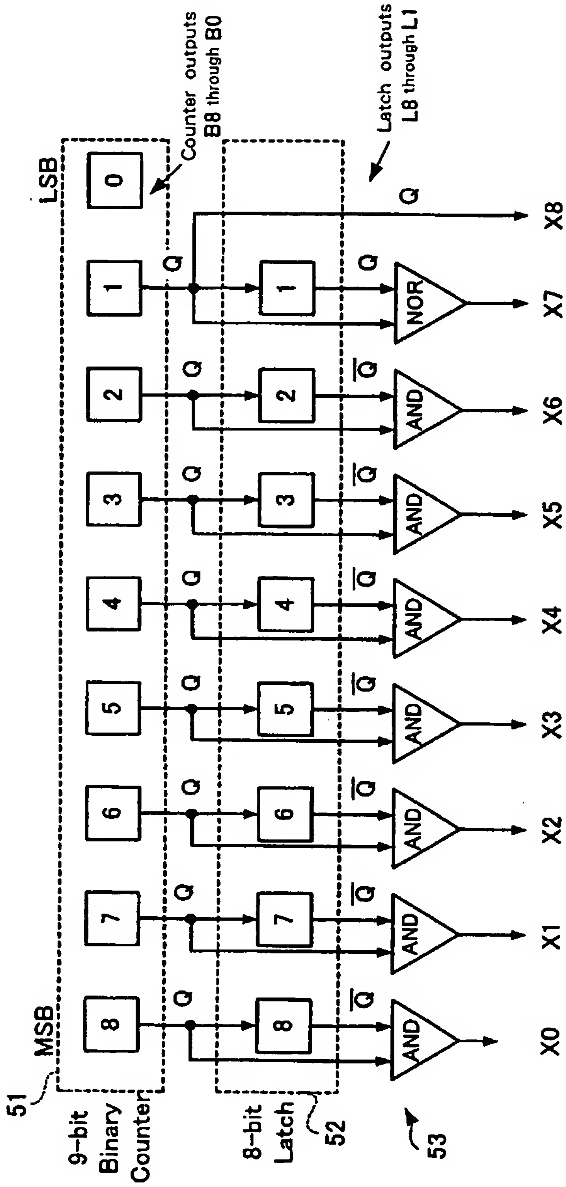

LSB
MSB
0
1
2
3
4
5
6
7
8
Q
Counter outputs
B8 through B0
Latch outputs
L8 through L1
NOR
AND
X0
X1
X2
X3
X4
X5
X6
X7
X8
51
9-bit
Binary
Counter
8-bit
Latch
52
53

Fig. 9

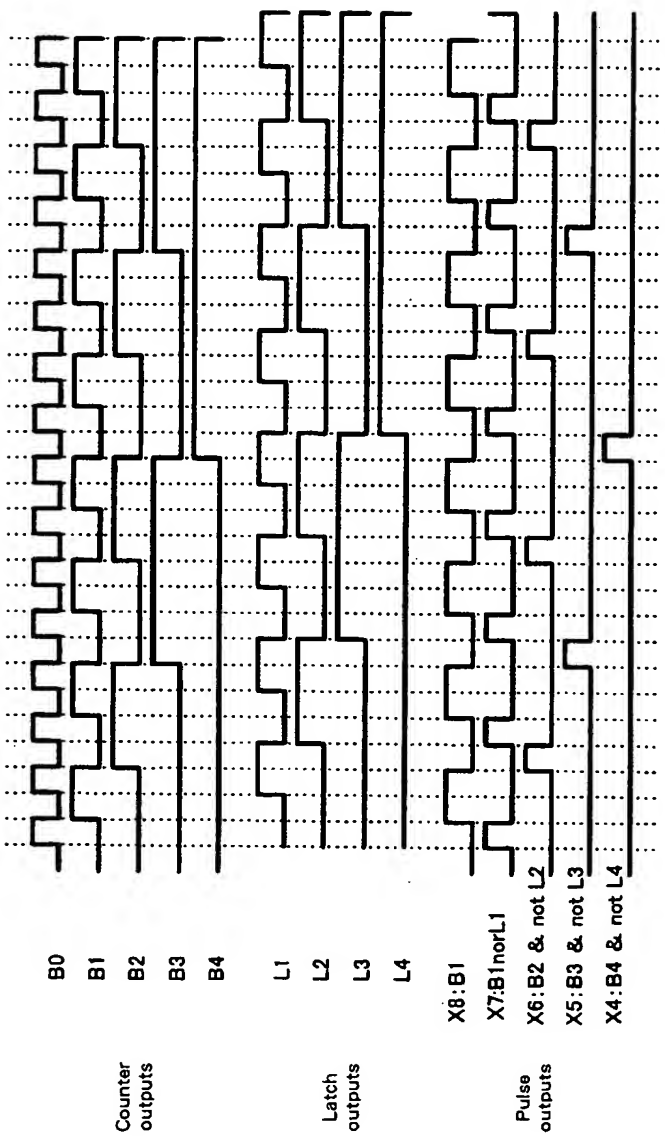


Fig. 10

Example pulse for PDM type DAC of the invention

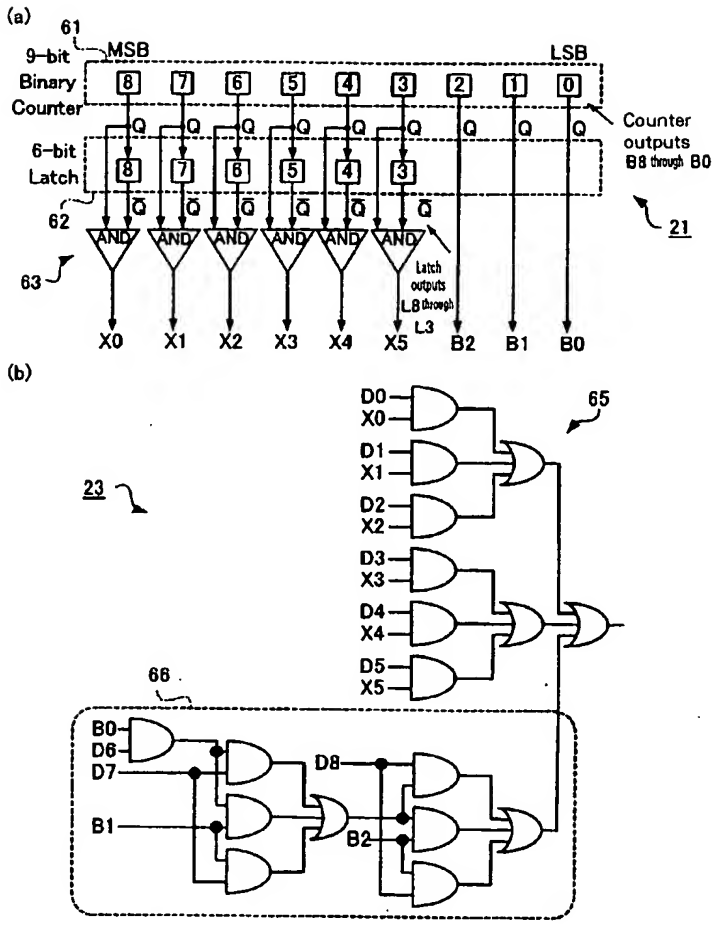
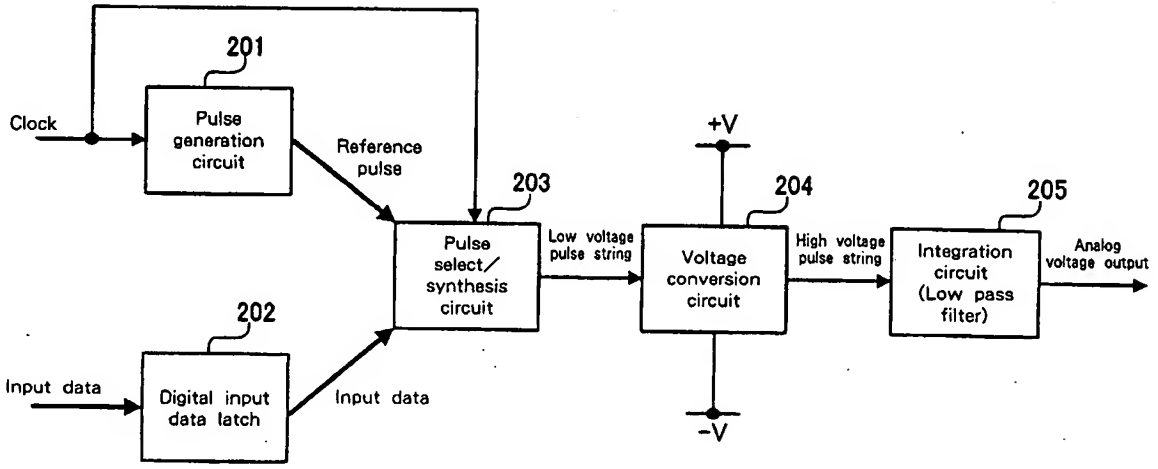


Fig. 11

Comparison of number of
gates between 4 clock unit and 8 clock unit

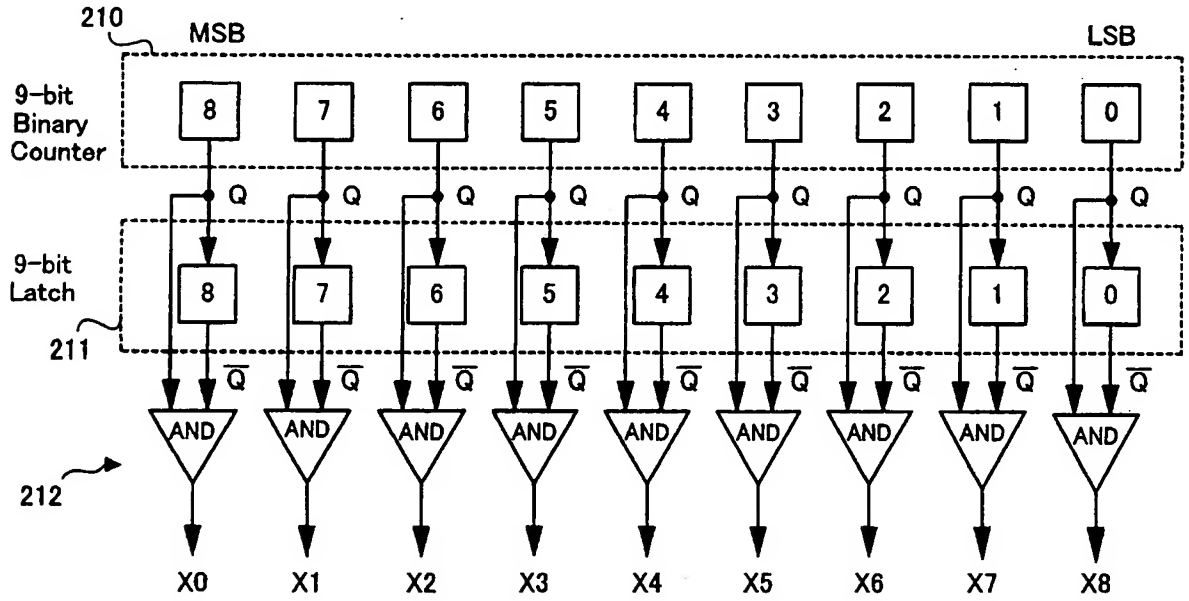
	4Clock	8Clock
Counter section		
Latch	17	15
2 – input AND	8	6
Pulse synthesis section (1 Set)		
2 – input AND	9	13
3 – input OR	4	5
Pulse synthesis section (10 Sets)		
2 – input AND	90	130
3 – input OR	40	50

Fig. 12



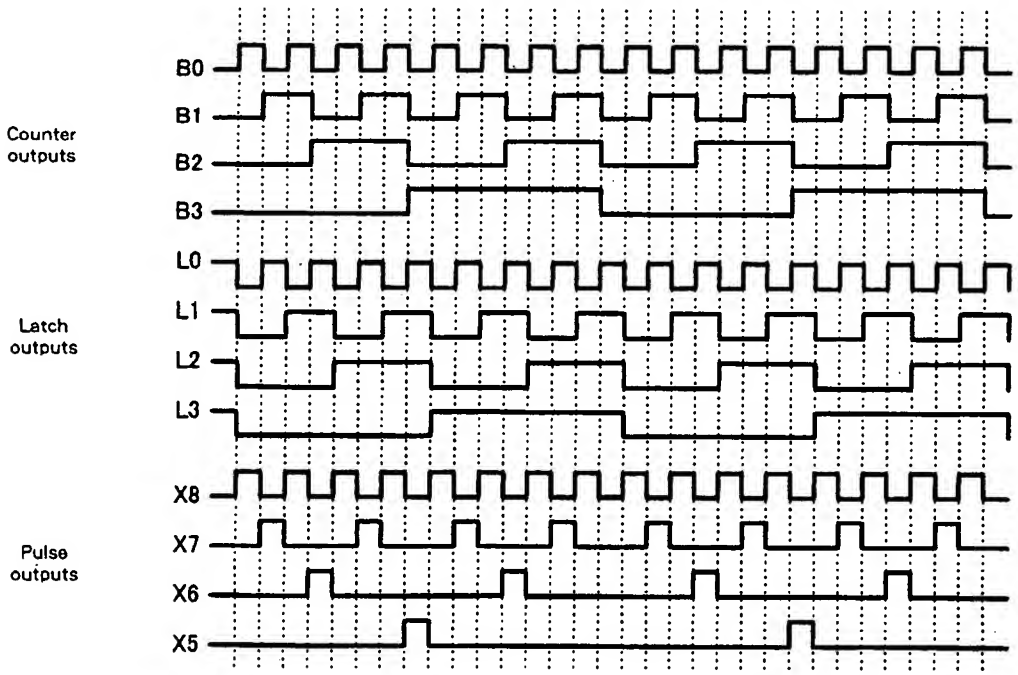
Configuration of PDM type DAC

Fig. 13



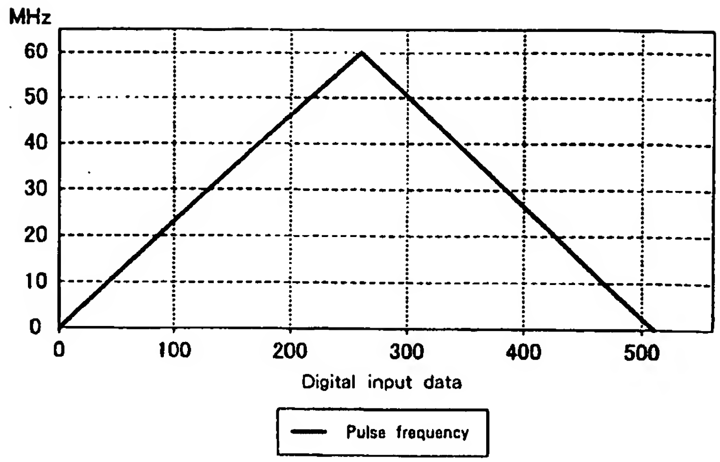
Configuration of pulse generation circuit for PDM type DAC

Fig. 14



Example pulse for PDM type DAC

Fig. 15



Pulse string frequency corresponding to each data

Fig. 16